inova® Semiconductors

Preliminary Data Sheet

APIX® Automotive Pixel Link

Digital Automotive Pixel Link

INAP125R12
INAP125R24
INAP125T12
INAP125T24

APIX is a new serial Gbit/s link for in-car infotainment and driver assistance systems. It features full-duplex pixel and sideband data transmission over one single pair of a shielded twisted pair (STP) copper cable. The downlink channel provides a sustained data rate of up to 1 Gbit/s, another 18 Mbit/s can be transmitted simultaneously in uplink direction. Alternatively, the uplink channel can also be established through a separate link to e.g. support transmission over fibre optic cable.

The APIX link is designed for the direct connection of high resolution TFT displays and CMOS image sensors to central graphic and image processors. The parallel interface of the APIX devices can be configured individually to match all popular display and image sensor interfaces.

Featuring a unique, asynchronous clock system, APIX links can also be cascaded to form loss-free distributed video networks in the car. Dedicated high-speed outputs with adjustable drive current and pre-emphasis in combination with spread-spectrum clocking facilitate the adaptation to different link distances and cable qualities while offering maximum data integrity and full EMI compliance.

Features:
- Low EMI, Two- or Four-Wire Full Duplex Link
- Up to 1 Gbit/s Downstream Link Bandwidth
- Up to 62.5 Mbit/s max Upstream Link Bandwidth
- 15 m+ Distance with low profile STP cables
- Tx/Rx: 10/12/18/24 bit RGB Interface
- DC-balanced line coding to support AC coupling
- Line Driver Current and Pre-Emphasis adjustable
- MicroWire® compatible Interface for Link configuration
- Extended Temperature Range: -40 to +105°C

Packages:
- 48/52/64 pin QFN (Quad-Flat No-Leads)

Applications:
- In-Car Information Displays
- Automotive Dashboard Displays
- Head-Up Displays
- Rear-Seat Infotainment
- Automotive Vision Systems
  - Lane Departure Warning
  - Obstacle Detection
  - Sign Recognition
  - Rear & Side Mirror Replacement
  - Blind Spot Detection
- Passenger Infotainment Systems
- Security Systems
- Machine Vision
- Military Head-Up and Helmet Displays

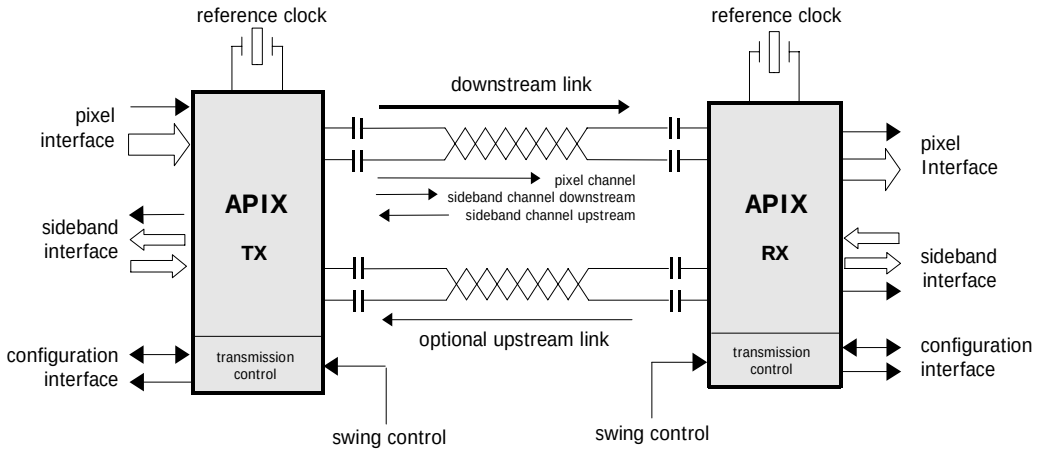

Figure 1: APIX Pixel Link Overview

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1 Introduction

The APIX link transmits uncompressed pixel data with a sustained and resolution-independent data rate of 1 Gbit/s (0.5 Gbit/s) over one single pair of STP copper cable. In addition to the pixel data, bi-directional sideband control data with a data rate of up to 62.5 Mbit/s can be transmitted over the same pair of cable.

The link supports distances of up to 15 m+ depending on the output settings (current, pre-emphasis) and the quality of the STP cable used.

The APIX chip features a flexible interface that can be configured for specific applications. These include the camera link from CMOS image sensors to a display/image processing unit, or the display link from a graphics processor to displays in the dashboard or rear seats.

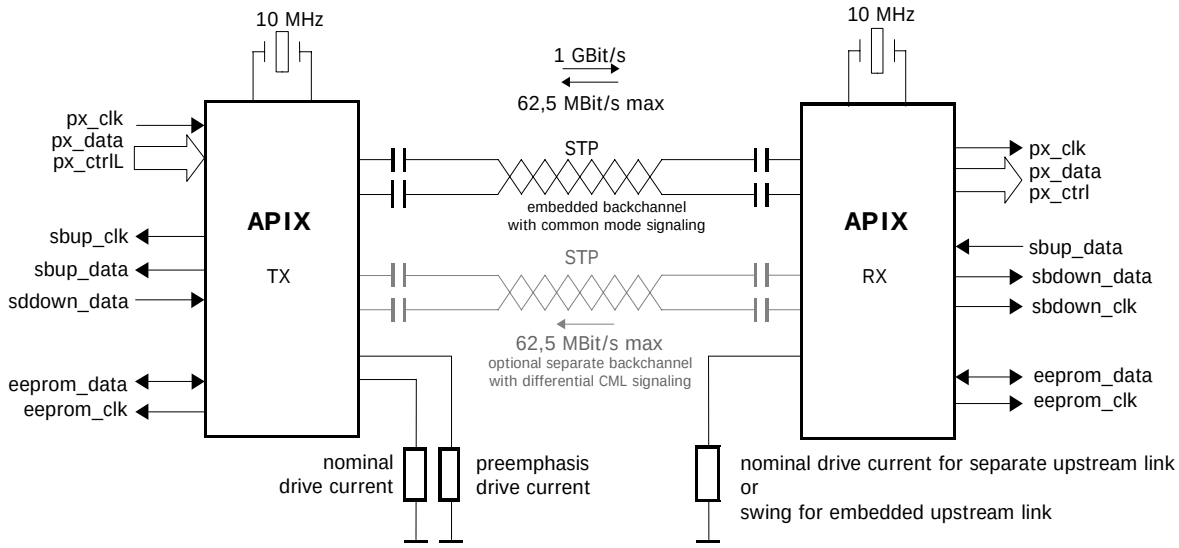


Figure 2: APIX Link Interfaces & Controls

1.1 Link Bandwidth

The physical connection between the Tx and Rx APIX devices is established by a single pair of STP copper cable carrying the downstream channels (pixel and control data) and the upstream channel (control data).

As an option, the APIX devices can also be configured to transmit the upstream data (back channel) over a separate pair of STP copper cable.

The bandwidth of the downstream link can be selected from these two modes:

- “full bandwidth” mode with a data rate of 1 Gbit/s for high-resolution, full colour display links
- “half bandwidth” mode with a data rate of 0.5 Gbit/s for camera links

The upstream link provides a net bandwidth of 62.5 Mbit/s, 41.7 Mbit/s, 31.3 Mbit/s or 20.8 Mbit/s (see table 1).

1.2 Transmission Channels

The APIX link provides three independent channels for data transfer: the uni-directional pixel channel (1 x downstream) and the bi-directional sideband channels for control data (1 x downstream, 1 x upstream).

The pixel channel and the downstream sideband channel are multiplexed and commonly transmitted over the downstream link.

The upstream sideband channel can either be established over the same pair of cable as the downstream link (embedded back channel) or alternatively over a separate pair of cable.

Channels	Full Bandwidth Mode (@ 10 MHz Ref. Clock)	Half Bandwidth Mode (@ 10 MHz Ref. Clock)
Downstream	**max. px_clk**	**max px_clk**
10 bit px_data	62 MHz	31 MHz
12 bit px_data	61 MHz	30.5 MHz
18 bit px_data	42 MHz	21 MHz
24 bit px_data	32 MHz	16 MHz
Sideband Channel	2 x 1 bit @ 12 Mbit/s max.	2 x 1 bit @ 6 Mbit/s max.
Upstream		
Sideband Channel	2 x 1 bit @ 9 Mbit/s max.	

Table 1: Bandwidth of upstream/downstream channels

2 APIX Transmitter

2.1 Interfaces

2.1.1 Downstream Link Interface

The interface of the downstream serial link (Tx -> Rx) is realized with differential Current Mode Logic (CML).

2.1.2 Upstream Link Interface

As the upstream serial channel (from Rx to Tx) can alternatively be established over the downlink (embedded back channel) or a separate pair of STP cable, different signaling techniques will be employed.

Option 1: Upstream and downstream channels share the same pair of STP cable. The upstream link employs common mode signaling technique.

Option 2: Upstream and downstream channels are transmitted over 2 separate pairs of STP cable. The additional upstream interface of the APIX devices is realized with differential Current Mode Logic (CML).

2.1.3 Pixel Channel Interface

Up to 24 bit of parallel pixel data representing the pixel RGB values is received via the pixel interface. The parallel pixel interface supports pixel formats of 10, 12, 18 and 24 bit. Pixel data and control signals are combined with the pixel interface clock. The active edge can be configured to either rising or falling. The logic level of this interface is 3.3 V.

2.1.4 Sideband Channel Downstream Interface

The sideband data downstream interface provides one 2-bit wide data input* where 2 bits of data are sampled.

2.1.5 Sideband Channel Upstream Interface

The sideband data upstream interface provides one 2-bit wide data output* where 2 bits of data are provided together with the corresponding clock.

* Depending on the APIX device used, only one 1-bit sideband channel may be available (see chapter 7 “Package Options”).

2.1.6 Signal Description

Signal Name	Direction	Description
px_data[23…0]	IN	24 bit of RGB pixel data
px_clk	IN	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of pxClk.
px_ctrl[2…0]	IN	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid. Displays: px_ctrl[0]: hsync; px_ctrl[1]: vsync; px_ctrl[2]: de
sbdown_data[1…0]	IN	Data sideband channel downstream
sbup_data[1…0]	OUT	Data sideband channel upstream
sbup_clk	OUT	Sideband channel upstream clock
reset_n	IN	Asynchronous reset
tx_error	OUT	Error indicator
eeprom_data	IN/OUT	Configuration data
eeprom_clk	OUT	Configuration clock
xtal_in	IN	Oscillator input or reference clock input
xtal_out	OUT	Oscillator output
nom_cur	PASSIV	Serial data downstream: nominal current control
pre_cur	PASSIV	Serial data downstream: pre-emphasis current control
sdout_p	OUT	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
sdout_n	OUT	
sdin_p	IN	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
sdin_n	IN	
vdd_vco	IN	Regulated power supply for VCO 1.8 V, 7 mA
vco_tune_in	IN	VCO loop filter tuning voltage
pfd_out	OUT	Current output for VCO loop filter
vdd	PWR	1.8 V core supply
dvdd	PWR	3.3 V I/O supply
vss	PWR	Digital core ground
dvss	PWR	Digital I/O ground
vdda	PWR	1.8 V analog supply
gnda	PWR	Analog ground
vdd_osc	PWR	1.8 V oscillator supply
dvdd_osc	PWR	3.3 V oscillator supply
vss_osc	PWR	Oscillator ground
dvss_osc	PWR	Oscillator I/O ground

Table 2: Transmitter signal description

3 APIX Receiver

3.1 Interfaces

3.1.1 Downstream Link Interface

The input of the serial link is realized with Current Mode Logic (CML). An analog equalizer is provided to pre-process the incoming serial signal.

3.1.2 Upstream Link Interface

APIX offers two options to establish the upstream link (see 2.1.2) . The upstream link can also be fully disabled.

3.1.3 Pixel Channel Interface

Up to 24 bit of parallel pixel data representing the pixel RGB values are provided at the pixel interface. The parallel pixel interface supports pixel formats of 10, 12, 18 and 24 bits. Pixel data and control signals are provided with reference to the pixel interface clock. The active edge can be set to either rising or falling. Pixel clock jitter is better than 1 ns. The interface has 3.3 V CMOS logic levels.

3.1.4 Sideband Channel Downstream Interface

The sideband data downstream interface provides one 2-bit wide data output* where 2 bits of data are provided together with the corresponding clock.

3.1.5 Sideband Channel Upstream Interface

The sideband data upstream interface provides one 2-bit wide data input* where 2 bits of data are sampled.

* Depending on the APIX device used, only one 1-bit sideband channel may be available (see chapter 7 “Package Options”).

3.1.6 Signal Description

Signal Name	Direction	Description
px_data[23…0]	OUT	24 bit of RGB pixel data if parallel mode
px_clk	OUT	Pixel data and pixel control signals are sampled with respect to the rising or falling edge of pxClk (parallel mode)
px_ctrl[2…0]	OUT	Pixel control signals, such as hsync, vsync, de or lineSync, frameSync, valid. Displays: px_ctrl[0]: hsync; px_ctrl[1]: vsync; px_ctrl[2]: de
sbup_data[1…0]	IN	Data sideband channel upstream
sbdown_data[1…0]	OUT	Data sideband channel downstream
sbdown_clk	OUT	Sideband channel downstream clock
reset_n	IN	Asynchronous reset
rx_error	OUT	Upstream Link error indicator
eeprom_data	IN/OUT	Configuration data
eeprom_clk	OUT	Configuration clock
xtal_in	IN	Oscillator input or reference clock input
xtal_out	OUT	Oscillator output
px_vco_in	IN	VCO for pixel clock generation – Input
px_vco_out	OUT	VCO for pixel clock generation – Output
swing	PASSIV	Upstream channel: nominal current control
sdout_n sdout_p	OUT OUT	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
sdin_p sdin_n	IN IN	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
vdd_vco	IN	Regulated power supply for VCO 1.8 V, 7 mA
vco_tune_in	IN	VCO loop filter tuning voltage
pfd_out	OUT	Current output for VCO loop filter
vdd	PWR	1.8 V core supply
dvdd	PWR	3.3 V I/O supply
vss	PWR	Digital core ground
dvss	PWR	Digital I/O ground
vdda	PWR	1.8 V analog supply
gnda	PWR	Analog ground
vdd_osc	PWR	1.8 V oscillator supply
dvdd_osc	PWR	3.3 V oscillator supply
vss_osc	PWR	Oscillator ground
dvss_osc	PWR	Oscillator I/O ground

Table 3: Receiver signal description

4 Configuration and Reset

Asynchronous reset can be activated at any time and sets the devices to a defined state. The device parameters and settings are configured through a two-wire serial interface which is compatible to the Microchip MicroWire® interface.

4.1 Tx Configuration Settings

Address (hex)	Bit #	Parameter	Recommended configuration value	Comment
00	7:0	PROM start	1011_1101	PROM valid byte 0
01	2:0	pre-emphasis control	000	
	3	dedicated upstream		0: disable 1: enable dedicated upstream link Note: in case bit 3 and 4 are set to '1', the upstream channel is disabled
	4	embedded upstream		0: disable 1: enable Note: in case bit 3 and 4 are set to '1', the upstream channel is disabled
	5	wobble		wobble of transmission frequency 0: disable 1: enable
	6	bandwidth mode		0: full rate 1: half rate
	7	wait period after configuration	1	0: no delay 1: 50 ms delay after configuration to stabilize the PLL
02	1:0	pixel data width		selects the width of pixel data to be transmitted 00: 10 bit 10: 18 bit 01: 12 bit 11: 24 bit
	4:2	reserved	110	Reserved
	5	pixel clock active edge		0: falling edge 1: rising edge
	7:6	upstream link serial clock		For detailed information refer to chapter 4.3.2
03	3:0	upstream link retiming control		For detailed information refer to chapter 4.3.3
	7:4	reserved	0000	Reserved
04	0	pll status		loss of PLL synchronization resets device 0: enable 1: disable
	4:1	reserved	1000	Reserved
	7:5	reserved	101	Reserved
05	7:0	PROM end	1001_1001	PROM valid byte 1

Table 4: Configuration of the Tx device

4.2 Rx Configuration Settings

Address (hex)	Bit #	Parameter	Recommended configuration value	Comment
00	7:0	PROM start	1011_1101	PROM valid byte 0
01	0	reserved	1	
	1	pixel interface wake-up 1		0: force pixel interface to “0” until VCO is stable 1: pixel interface is always enabled
	2	equalizer		0: enable equalizer 1: disable equalizer
	3	dedicated upstream		0: disable 1: enable dedicated upstream link Note: in case bits 3 and 4 are set to '1', the upstream channel is disabled
	4	embedded upstream		0: disable 1: enable Note: in case bits 3 and 4 are set to '1', the upstream channel is disabled
	5	reserved	0	reserved
	6	bandwidth mode		0: full rate 1: half rate
	7	wait period after configuration	1	0: no delay 1: 50 ms delay after configuration to stabilize the PLL
02	1:0	pixel data width		00: 10 bit 01: 12 bit 10: 18 bit 11: 24 bit
	4:2	reserved	110	reserved
	5	pixel clock active edge		0: falling edge 1: rising edge
	7:6	upstream link serial clock		For detailed information refer to chapter 4.3.2
03	0	unused	0	
	1	pixel interface wake-up 2		px_data and px_ctrl start at the upper left corner 0: disable 1: enable
	2	pixel interface wake-up 3		px_clk starts at the upper left corner 0: disable 1: enable
	3	fault tolerant transmission	1	tolerates single bit errors within the timing window 0: disable 1: enable
	7:4	reserved	0000	reserved
04	0	pll status	0	loss of PLL synchronization resets device 0: enable 1: disable
	7:1	reserved	00000	
05	7:0	reserved	00000000	reserved
06	7:0	reserved	00000000	reserved
07	7:0	PROM end	1001_1001	PROM valid byte 1

Table 5: Configuration of the Rx device

4.3 Configuration of the Sideband Upstream Channel's Clock System

4.3.1 General Information

The sideband upstream interface supports different levels of transmission bandwidth selected through configuration settings. The following descriptions always are valid, no matter if the embedded (= one-pair cable link) or external (= two-pair cable link) upstream channel is used.

4.3.2 Selection of Transmission Bandwidth

4.3.2.1 Configuration for Full Bandwidth Mode (1 Gbit/s)

Bandwidth mode	Tx upstream link serial clock	Rx upstream link serial clock	Upstream link bandwidth	Rx sideband upstream channel max data rate
full rate	00	01	62,5 MBit/s	2 x 9 MBit/s
full rate	01	10	41,67 MBit/s	2 x 6 MBit/s
full rate	10	11	31,25 MBit/s	2 x 4 MBit/s

Table 6: Sideband upstream configuration for full bandwidth mode

4.3.2.2 Configuration for Half Bandwidth Mode (0.5 Gbit/s)

Bandwidth mode	Tx upstream link serial clock	Rx upstream link serial clock	Upstream link bandwidth	Rx sideband upstream channel max data rate
half rate	00	00	62,5 MBit/s	2 x 9 MBit/s
half rate	01	01	31,25 MBit/s	2 x 6 MBit/s
half rate	11	10	20,83 MBit/s	2 x 2.5 MBit/s

Table 7: Sideband upstream configuration for half bandwidth mode

4.3.3 Retiming Control of Upstream Link

The following parameter settings for “upstream link retiming control” are recommended for proper retiming of the serial signal.

Configuration Parameters			
Bandwidth mode	**Tx upstream link serial clock**	**Rx upstream link serial clock**	**Upstream link retiming control**
full rate	00	01	0011
full rate	01	10	0001
full rate	10	11	0011
half rate	00	00	0011
half rate	01	01	0011
half rate	11	10	0111

Table 8: Configuration of upstream link retiming control

4.4 APIX Configuration Procedure

For the configuration of all parameters, the APIX device provides a MicroWire® compatible two-wire interface. Recommended EEPROMs are e.g. 93L46A or 93L46C by Microchip Technology Inc. The following diagram provides the configuration flow:

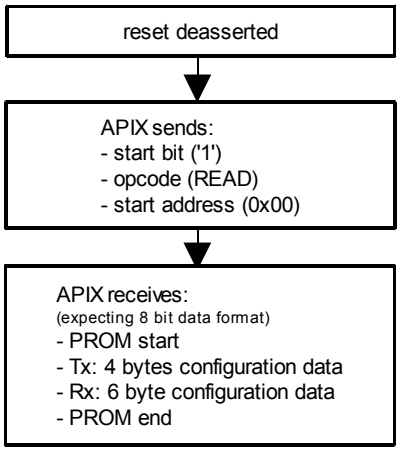


Figure 3: Configuration flow

Note: In case of invalid “PROM start” or “PROM end” bytes, a default configuration is used.

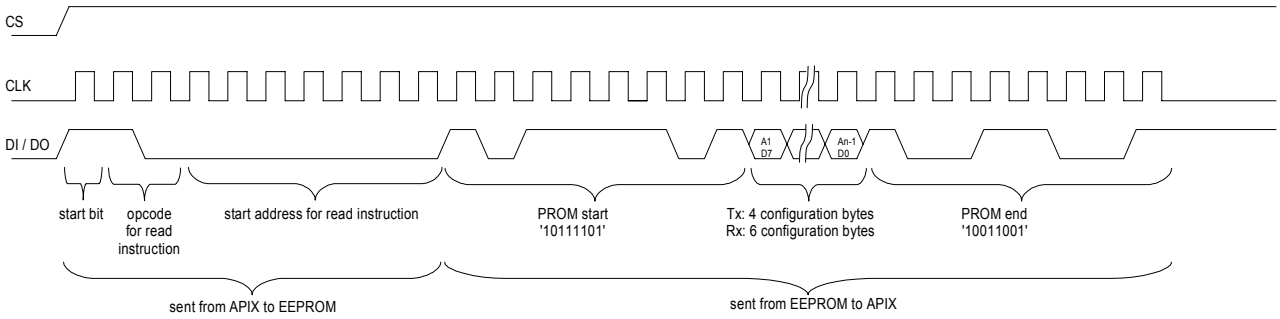


Figure 4: Configuration sequence

The following schematic shows the external configuration circuitry using EEPROM 93LC46A-P:

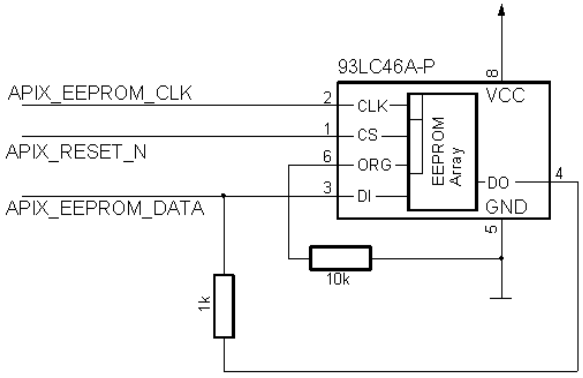


Figure 5: External configuration circuit

5 Electrical Specification

5.1 External Circuits

5.1.1 External Loop Filter Specification

The APIX PLL circuits require an external RC loop filter. **Figure 5** shows the external loop filter circuit for the core VCO. **Figure 6** shows the circuit for the pixel clock VCO.

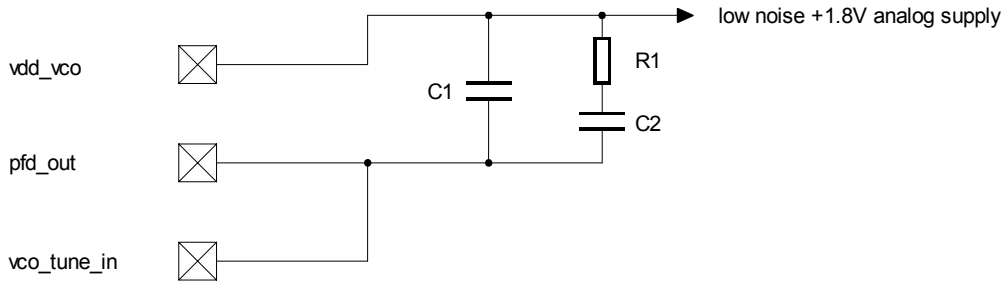


Figure 6: External loop filter circuit for system clk VCO

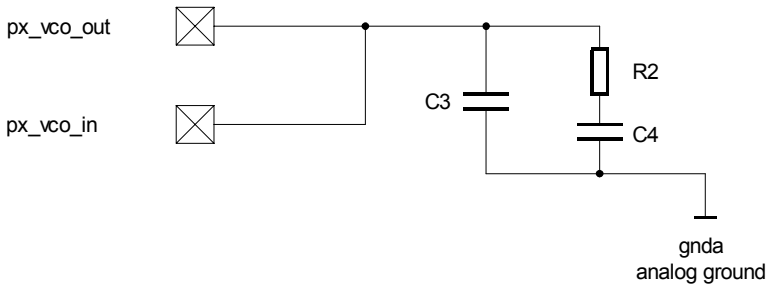


Figure 7: External loop filter circuit for pixel clock VCO at Rx

Table 9 shows the component values for the system clock VCO loop filter and for the pixel clock VCO loop filter. The use of SMD ceramic chip capacitors and chip resistors is recommended.

VCO	Signals	Parameter	Symbol	Value Tx	Value Rx	Units
core VCO	vdd_vco pfd_out vco_tune_in	Loop Filter Capacitor C_1	C_1	1,5	10	nF
		Loop Filter Capacitor C_2	C_2	10	10	nF
		Loop Filter Resistor R_1	R_1	220	100	kΩ
px clk VCO	px_vco_out px_vco_in	Loop Filter Capacitor C_3	C_3	-	2	nF
		Loop Filter Capacitor C_4	C_4	-	47	nF
		Loop Filter Resistor R_2	R_2	-	1	kΩ

Table 9: Loop filter values for system clk VCO and pixel clk VCO

5.1.2 External Reference Clock Circuit

The APIX core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal (Figure 8). Alternatively a stable 10 MHz clock signal (3.3 V CMOS TTL) can directly be connected to pin 'xtal_in' with 'xtal_out' left open.

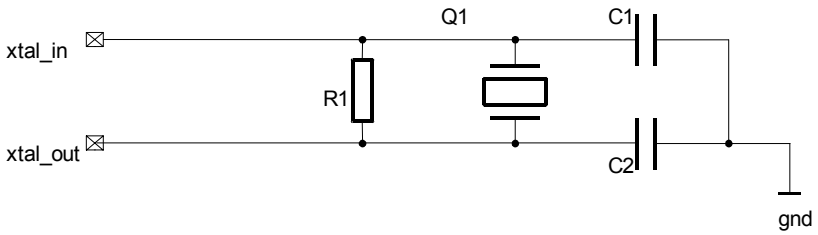


Figure 8: Oscillator reference circuit

Reference Clock Source	Signals	Parameter	Symbol	Value Tx	Value Rx	Units
clock oscillator	xtal_in xtal_out	clock oscillator	Q_1	10	10	MHz
		resistor	R_1	2	2	MΩ
		capacitor	C_1	33	33	pF
			C_2	33	33	pF
3.3 V TTL	xtal_in	3.3 V TTL clock signal	-	10	10	MHz
	xtal_out	unconnected	-	-	-	-

Table 10: Values for reference clock circuitry

5.1.3 Reference Circuit of the Nominal and Pre-Emphasis Current (Tx)

For optimized signal integrity and lowest EMI in dependence of the quality and length of the STP cable used, the output nominal current and the pre-emphasis current of the APIX Tx device can be set individually by means of external resistors.

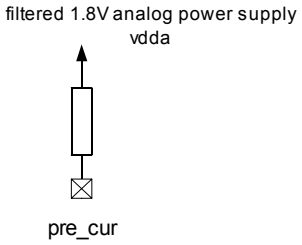


Figure 8: Pre-emphasis current

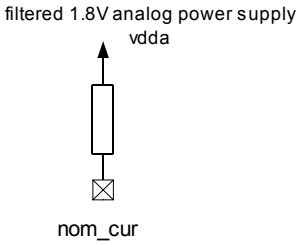


Figure 9: Nominal current

Pin Name	R_{pre_cur}, R_{nom_cur}		Units
	min	max	
nom_cur	250	10000	Ω
pre_cur	250	10000	Ω

Table 11: Component values for nominal and pre-emphasis current

5.1.4 Reference Circuit of the Swing Control (Rx)

To achieve optimum transmission of the upstream link, the signal swing of the Rx device can be adjusted by means of an external resistor. When using the embedded upstream channel, the resistor controls the swing amplitude. When using the external upstream link, the resistor adjusts the nominal drive current.

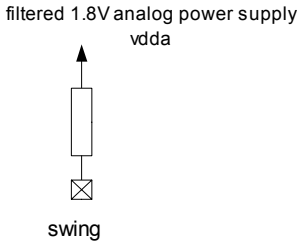


Figure 9: Rx nominal current

Pin Name	R_{nom_cur}		Units
	min	max	
swing	250	10000	Ω

Table 12: Component value for Rx nominal current / swing

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors is not liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	t.b.d.	t.b.d.	V	
Input Voltage	V_{IN}	t.b.d.	t.b.d.		
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Junction Temperature (under bias)	T_j	-45	+140	° C	
Storage Temperature	T_{stg}	-55	+150	° C	
Soldering Temp./Time	T_{SLD} / T_{SLD}		t.b.d.		
Static Discharge Voltage (CMOS dig. I/O vs. respective GND & Supply rails)	V_{SDCMOS}		t.b.d.	V	Human Body Model
Static Discharge Voltage (all other pin combinations including CML I/O pins)	V_{SDCML}		t.b.d.	V	Human Body Model

Table 13: Absolute maximum ratings

6.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage Core	V_{CC_CORE}	1.71	1.89	V	1.8 V ± 5%
DC Supply Voltage IO	V_{CC_IO}	3.15	3.45	V	3.3 V ± 5%
CML Output Current	I_{OUTCML}	0.8	24	mA	
Junction Temperature (under bias)	T_j	-40	+125	° C	
Ambient Temperature	T_a	-40	+105	° C	

Table 14: Recommended operating conditions

6.3 DC Characteristics (under recommended operating conditions)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CMOS Input High Voltage	V_{IH}	Vcc = 3.3 V	2.0			V
CMOS Input Low Voltage	V_{IL}	Vcc = 3.3 V	0		0.8	V
CMOS Input High Current	I_{IH}	V_{IN} = Vcc	-10		10	µA
CMOS Input Low Current	I_{IL}	V_{IN} = 0 V	-15		-77	µA
CMOS Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4			V
CMOS Output Low Voltage	V_{OL}	I_{OL} = 4 mA			0.4	V
CMOS Output High Current	I_{OH}	V_{OH} = 0.9 x Vcc			4	mA
CMOS Output Low Current	I_{OL}	V_{OL} = 0.1 x Vcc			-4	mA
Power Dissipation Tx	P_{max_Tx}	max data transmission rate		170		mW
Power Dissipation Rx	P_{max_Rx}	max data transmission rate		220		mW

Table 15: DC characteristics

Note: Floating CMOS inputs can result in excessive supply current. Therefore, unused inputs should be tied to Vcc or GND.

6.4 AC–Characteristics

Parameter	Min.	Typ.	Max.	Units
Input Capacitance, any pin		3	5	pF
Serial Transmission Gross Data Rate (Downstream)	500		1000	Mbit/s
Serial Transmission Net Data Rate (Upstream)		18		Mbit/s
CMOS Output Rise / Fall Time (C_L = 10 pF)		5	10	ns

Table 16: AC characteristics

6.5 Reference Clock Specification (T_a = -40 to +105° C; V_{cc} = 1.71 - 1.89V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Nominal Frequency	f_{OSC}	t.b.d.	10	t.b.d.	MHz	
Frequency Tolerance	F_{TOL}	-100		+100	ppm	

Table 17: Reference clock specification

7 Package Options / Pinouts / Package Dimensions

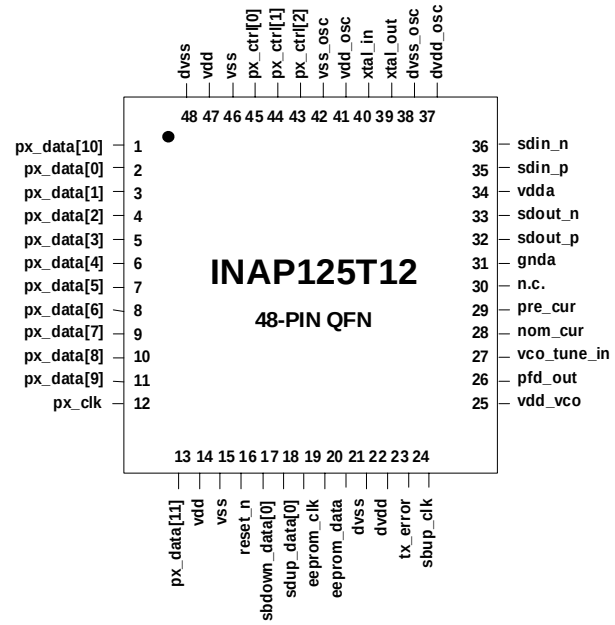
7.1 Package Options / Ordering Codes

To reduce pin count and save board space, the APIX devices are available in different QFN package. All package options are fully RoHS-compliant.

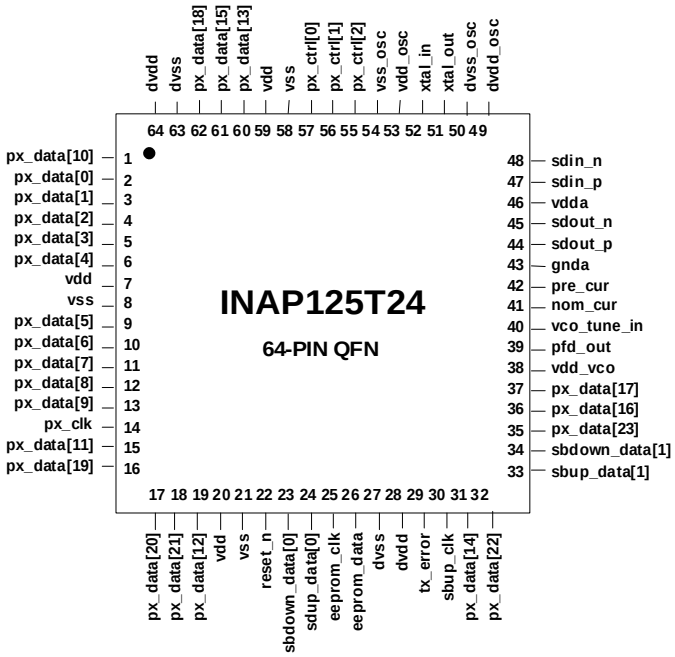
Device / Ordering Code	Description	Package	Package Quantity
Transmitter			
INAP125T12	Tx incl. 10...12 bit Interface + 1 bit Sideband	QFN48	416pcs/tray
INAP125T24	Tx incl. 10...24 bit Interface + 2 bit Sideband	QFN64	260pcs/tray
Receiver			
INAP125R12	Rx incl. 10...12 bit Interface + 1 bit Sideband	QFN52	260pcs/tray
INAP125R24	Rx incl. 10…24 bit Interface + 2 bit Sideband	QFN64	260pcs/tray

7.2 Pinouts

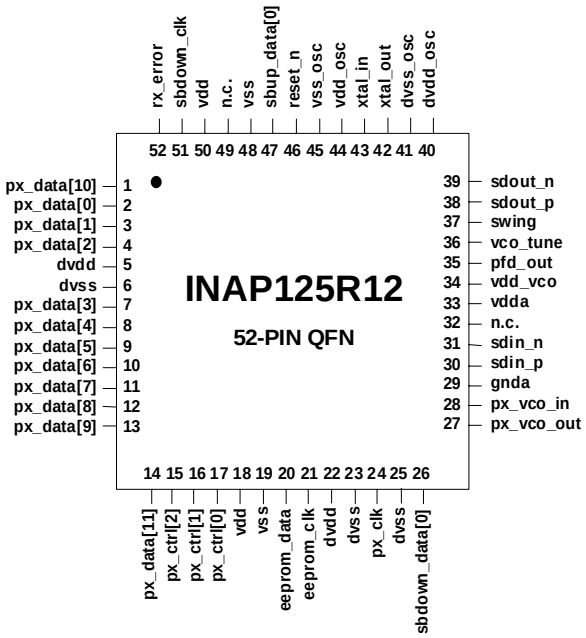
7.2.1 APIX Transmitter INAP125T12



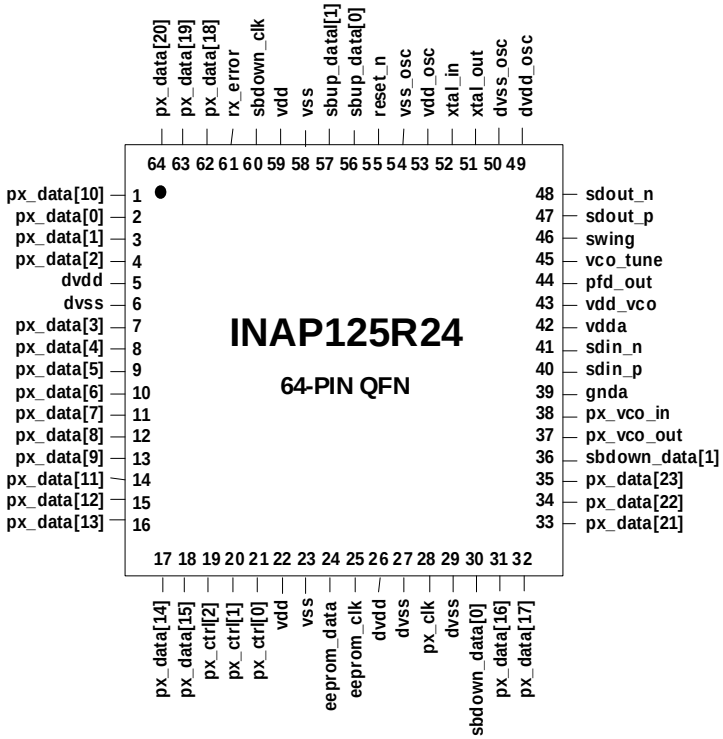
7.2.2 APIX Transmitter INAP125T24



7.2.3 APIX Receiver INAP125R12

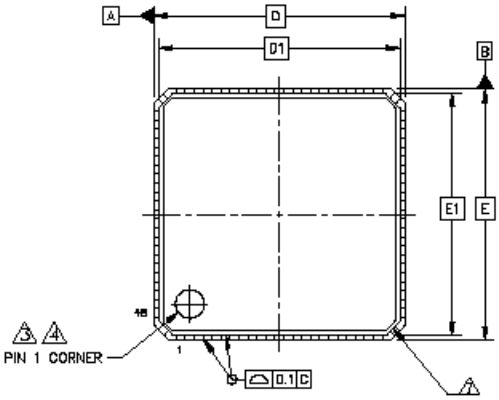


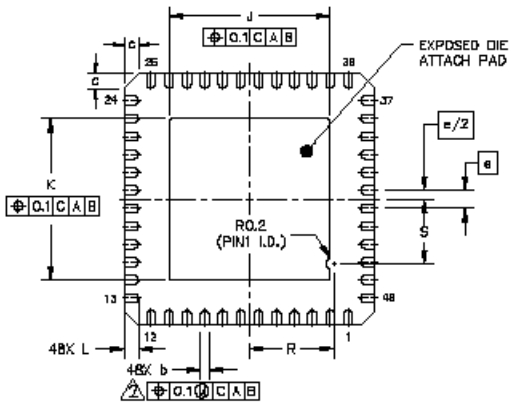
7.2.4 APIX Receiver INAP125R24



7.3 Package Dimensions (all values in mm)

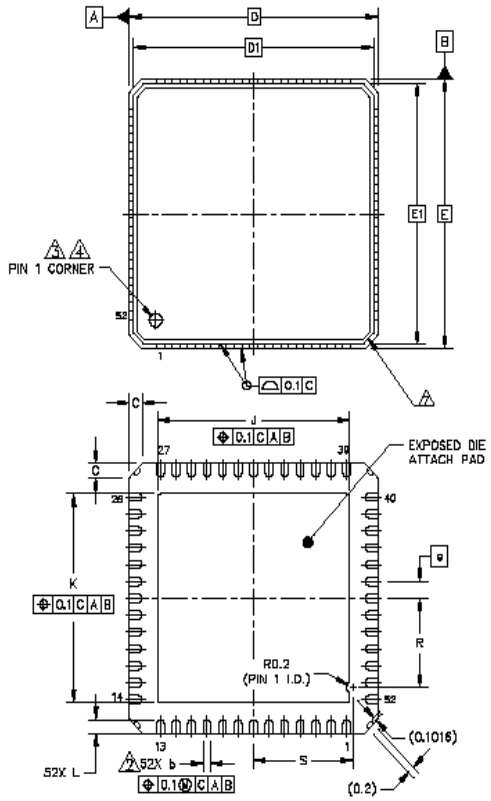
48-PIN QFN





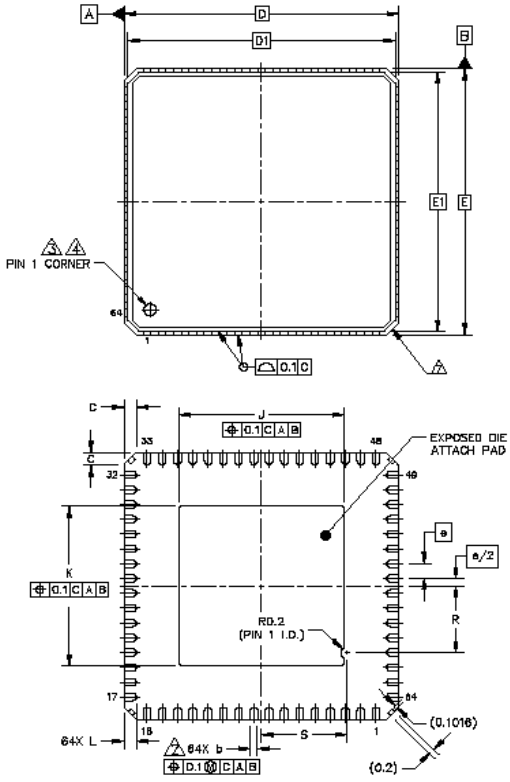
DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		7 BSC	
D1		6.75 BSC	
E		7 BSC	
E1		6.75 BSC	
e		0.5 BSC	
J	4.4	4.5	4.6
K	4.4	4.5	4.6
L	0.3	0.4	0.5
R	2.25	2.35	2.45
S	1.7	1.8	1.9

52-PIN QFN



DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		8 BSC	
D1		7.75 BSC	
E		8 BSC	
E1		7.75 BSC	
e		0.5 BSC	
J	6.1	6.2	6.3
K	6.1	6.2	6.3
L	0.3	0.4	0.5
R	2.55	2.65	2.75
S	3.1	3.2	3.3

64-PIN QFN



DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		9 BSC	
D1		8.75 BSC	
E		9 BSC	
E1		8.75 BSC	
e		0.5 BSC	
J	5.3	5.4	5.5
K	5.3	5.4	5.5
L	0.3	0.4	0.5
R	2.15	2.25	2.35
S	2.7	2.8	2.9

8 Revision History

- V 0.9 Initial *Preliminary Data Sheet*

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